What is claimed is:

[Claim 1] 1. A semiconductor integrated circuit, comprising:

a) a semiconductor-on-insulator (SOI) region with a buried dielectric layer;

b) a bulk semiconductor region adjacent to the SOI region;

c) a trench filled with epitaxial semiconductor material disposed between the SOI region and bulk region.

[Claim 2] 2. The semiconductor integrated circuit of claim 1 further comprising a buried sidewall spacer between the SOI region and bulk region, and disposed under the trench filled with epitaxial semiconductor material.

[Claim 3] 3. The semiconductor integrated circuit of claim 1 further comprising:

a) a first type doping in the bulk region;

b) a second type doping in the SOI region;

c) a butted P-N junction between the first-type doping and second type doping, wherein the butted junction is disposed in the SOI region, or in the filled trench.

[Claim 4] 4. The semiconductor integrated circuit of claim 3 wherein the first type doping extends into the SOI region.

[Claim 5] 5. The semiconductor integrated circuit of claim 3 wherein the trench filled with epitaxial semiconductor material has the first type doping.

[Claim 6] 6. The semiconductor integrated circuit of claim 3 further comprising a metal silicide layer disposed on the butted P-N junction.

[Claim 7] 7. The semiconductor integrated circuit of claim 6 wherein the metal silicide layer is disposed on a portion of the bulk region having the first type doping and on a portion of the SOI region having the second type doping.

[Claim 8] 8. The semiconductor integrated circuit of claim 1 wherein the SOI region and bulk region have different crystal orientations.

[Claim 9] 9. The semiconductor integrated circuit of claim 8 wherein the SOI region and bulk region are made of silicon, and wherein the SOI region has a {110} crystal orientation, and the bulk region has a {100} crystal orientation.

[Claim 10] 10. A semiconductor integrated circuit, comprising:

a) a semiconductor-on-insulator (SOI) region with a buried dielectric layer;

b) a bulk semiconductor region adjacent to the SOI region;

c) a P-N junction formed from a first type doping in the bulk region and a second type doping in the SOI region;

d) a metal silicide layer disposed on and electrically bridging the P-N junction.

[Claim 11] 11. The semiconductor integrated circuit of claim 10 wherein the P-N junction is disposed in the SOI region.

[Claim 12] 12. The semiconductor integrated circuit of claim 10 wherein the P-N junction is disposed at the trench filled with epitaxial semiconductor material.

[Claim 13] 13. The semiconductor integrated circuit of claim 10 further comprising a trench filled with epitaxial semiconductor material disposed between the SOI region and bulk region.

[Claim 14] 14. A method for forming a semiconductor integrated circuit with an SOI region and a bulk region, comprising the steps of:

a) forming a substrate with and SOI region and a bulk region separated by an embedded sidewall spacer;

b) etching the sidewall spacer to form an empty trench; and

c) epitaxially depositing semiconductor material in the trench.

[Claim 15] 15. The method of claim 14 further comprising the steps of:

d) planarizing the wafer after step (c); and

e) forming a first type doping in the bulk region, and a second type doping in the SOI region, wherein a P-N junction between the first type doping and the second type doping is disposed in the SOI region or in the trench.

[Claim 16] 16. The method of claim 15 further comprising the step of:

f) forming a metal silicide layer across the P-N junction after step (f).

[Claim 17] 17. The method of claim 13 wherein the sidewall spacer is completely removed in step (b).

[Claim 18] 18. The method of claim 13 wherein the sidewall spacer is partially removed in step (b).